Basic configurations of MOS transistor

4 B

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1. Introduction

This exercise enables measurement and comparison the parameters of the basic configurations of the bipolar transistor. These are respectively a common source circuit (CS), common gate (CG) and a common drain (CD). As an exercise, measurements are: gain in the middle of bandwidth, input and output resistance, the lower and upper 3dB cut-off frequency and amplitude frequency characteristics beyond the bandwidth of the amplifier. Different configurations are selected using a rotary switch, which, through relays, switches between the three configurations CS, CG and CD. The fourth position of the switch is used to short circuit signal from the input socket to the output. This enables the measurement of input and output voltage with the help of one and the same instrument. There are almost identical conditions of powering the transistors in different circuits. The differences between the parameters of the amplifiers are mainly due to the different operating configuration of the active element, enabling a qualitative comparison of the circuits. For independence from the parameters of measuring instruments and quality of the connections each amplifier has built-in buffer with the gain equal of 1.

Prior to the exercise, read the theory about the operation of the MOS transistor as a linear amplifier (posted in this paper).Teacher is obliged to check the preparation for the exercise.

2. Measurements

For each of the circuits CS, CG and CD:
a) determine the gain in the middle of bandwidth v_o/v_s (conditions: input signal frequency of 5kHz and input voltage about 30mV for CS and CG, for the CD circuit about 300mV).
b) determine the input resistance (the same input voltage, description in the theory part).

In order to determine the input resistance (with the constant input voltage):
- measure output voltage $\mathbf{v_o}$;
- open the $\mathbf{R_{SZER}}$ resistor (press and hold the R_{IN} button) and measure the new output voltage $\mathbf{v_o'}$;
- Determine the input resistance from the equation:

$$R_{IN} = \frac{v_o'}{v_o - v_o'} \cdot R_{SZER} - R_{GEN} \qquad (1)$$

c) determine the output resistance (input signal as in the a) point, description in the theory part).

In order to determine the output resistance (with the constant input voltage):
- measure output voltage $\mathbf{v_o}$;
- close the $\mathbf{R_{RÓW}}$ resistor (press and hold the R_{OUT} button) and measure the new output voltage $\mathbf{v_o'}$;
- Determine the output resistance from the equation:

$$R_{OUT} = \frac{R_L \parallel R_{BUF}\left(1 - \frac{v_0}{v_0'}\right)}{\frac{v_0}{v_0'} - \frac{R_L \parallel R_{BUF}}{R_L \parallel R_{BUF} \parallel R_{RÓW}}} \qquad (2)$$

d) measure the lower and upper 3dB cut-off frequency (f_{3dBL} , f_{3dBH}). The measurement should be performed as follows:
- set the frequency of the signal generator at 5kHz,
- set the input voltage so to get 300mV on the output
- reduce (for measuring the frequency of the lower limit) or increase (for frequency measurement upper limit), the frequency of the input signal until the output voltage will be equal to $300mV/\sqrt{2}$, the values obtained are appropriate cut-off frequencies.

e) measure the amplitude frequency characteristics in the range from 30Hz to f_{3dBL} and from f_{3dBH} to 2MHz in the grid of frequency of 1, 2, 4, 7, 10 (ie. eg. for 10Hz, 20Hz, 40Hz, 70Hz, 100Hz, ...). The measured characteristics should be plotted. The vertical axis should be gain expressed in the logarithmic measure, ie. $20\log_{10}|V_O/V_{IN}|$, othe horizontal axis (measurement signal frequency) should be logarithmic.

Examples of measurement tables

	CS	CG	CD
$\mathbf{V_o/V_{in}}$ [V/V]			
$\mathbf{R_{in}}$ [kΩ]			
$\mathbf{R_{out}}$ [kΩ]			
$\mathbf{f_{3dBL}}$ [Hz]			
$\mathbf{f_{3dBH}}$ [kHz]			

f [Hz]	30	40	...	f_{3dBL}	f_{3dBH}	...	1M	2M
$\mathbf{V_0/V_{IN}}$								

3. Description of results

For the circuits CS, CG and CD:
- operating points of transistors
- small signal gain v_o/v_{in},
- ower and upper 3dB cut-off frequency,
- input and output resistances

should be calculated theoretically.
The results of the calculations should be placed so that you can easily compare them with measurements (eg. In a common table). For each of the circuits plot the measured frequency characteristics of the gain module and apply to them the results of calculations (ie. The gains of the middle band and of the upper and lower cut-off frequencies). Place your own conclusions and observations. Compare deals between themselves and comment on compliance calculations with the measurements.

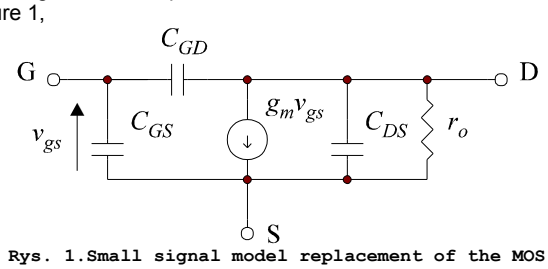
4. Theory

The exercise is made with three amplifiers labeled CS, CG and CD. All systems have built-in input and output buffers. These buffers are identical and their parameters are presented in the following table:

Parameter	Unit	Value
Gain	V/V	1
Input resistance R_{BUF}	MΩ	1

Output resistance R_{GEN}	Ω	50
Input capacitance C_{BUF}	pF	3
Cut-off frequency	MHz	4

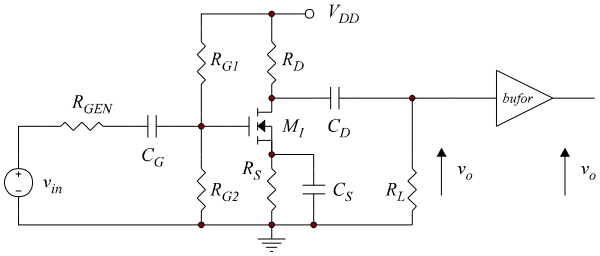
Small signal model replacement of the MOS transistor is shown in Figure 1,



Rys. 1.Small signal model replacement of the MOS transistor

where: $g_m = 2\sqrt{K_N I_D}$, $I_D = K_N (V_{GS} - V_T)^2$, $r_O = V_A / I_D$, V_T - threshold voltage $K_N = 0{,}5 k_n W/L$ - transconductance parameter of MOS transistor, *W, L* - width and length of the channel, k_n - the mobility of carriers in the channel. The parameters of transistors used in the exercise are given in the table at the end of the study. Due to the high value of V_A voltage or transistors used, the output resistance of MOS transistors in this exercise has been omitted.

4.1 Common Source circuit(CS):

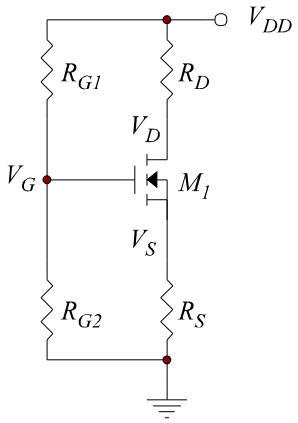


Rys. 2.Diagram of MOS transistor amplifier in the common source configuration (CS).

4.1.1 Operating point

Due to the lack of current flow through the gate of the MOS transistor voltage on their connection can be calculated using the formula for a voltage divider:

$$V_G = V_{DD} \frac{R_{G2}}{R_{G1} + R_{G2}} \tag{3}$$



Rys. 3.Diagram to determine the operating point of the transistor.

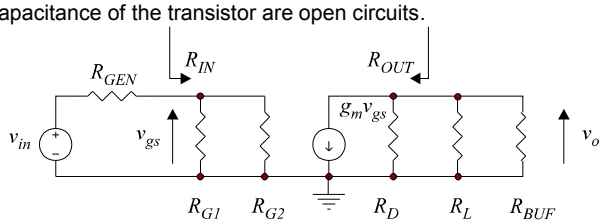
The voltage at source is equal to the voltage drop across the resistor R_S, hence the gate voltage - source can be expressed by the formula: $V_{GS} = V_G - I_D R_S$; while the drain current can be determined from the equations:

$$\begin{cases} V_{GS} = V_G - I_D R_S \\ I_D = K_N (V_{GS} - V_T)^2 \end{cases} \tag{4}$$

The solutions of the above equations are two different currents, the valid one satisfies the inequality: $V_{GS} = V_G - I_D R_S > V_T$. Knowing the value of the drain current the voltage at the source and the drain of of the MOS transistor can be determined by as: $V_S = I_D R_S$ and $V_D = V_{DD} - I_D R_D$. When the inequality is satisfied: $V_{DS} \geq V_{GS} - V_T$, the transistor operates in the saturation, and its transconductance is: $g_m = 2\sqrt{K_N I_D}$.

4.1.2 Small signal analysis

Middle of bandwidth:
Small signal model in the medium frequency range (bandpass) is formed assuming that the coupling capacitance and shunt constitute a short circuit for AC signal, while the parasitic capacitance of the transistor are open circuits.



Rys. 4.Small signal model of the amplifier circuit CS for medium frequency range.

$$R_{IN} = R_{G1} \parallel R_{G2} \tag{5}$$

$$R_{OUT} = R_D \tag{6}$$

$$v_0 = -g_m v_{gs} (R_D \parallel R_L \parallel R_{BUF}) \tag{7}$$

$$v_{gs} = \frac{R_{IN}}{R_{IN} + R_{GEN}} v_{in} \tag{8}$$

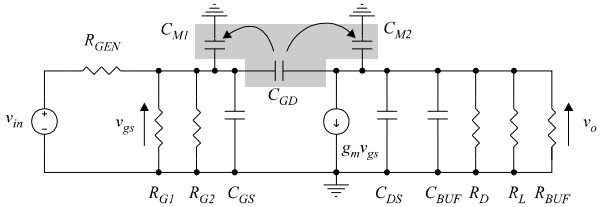
$$\frac{v_0}{v_{in}} = -\frac{R_{IN}}{R_{IN} + R_{GEN}} g_m (R_D \parallel R_L \parallel R_{BUF}) \tag{9}$$

High frequency
The upper cut-off frequency is determined based on the time constants, associated with the respective capacities parasitic of the MOS transistor. Using Miller Theorem capacitance C_{GD} can be exchanged (patrz rys. 5) with C_{M1} i C_{M2}.capacitances

$$K = \frac{v_o}{v_{gs}} = -g_m (R_D \parallel R_L \parallel R_{BUF}) \tag{10}$$

$$C_{M1} = C_{gd}(1 - K) \tag{11}$$

$$C_{M2} = C_{gd}\left(1 - \frac{1}{K}\right) \tag{12}$$



Rys. 5. Small signal model to determine the upper cut-off frequency.

After the C_{GD} exchange there are two time constants of the following values:

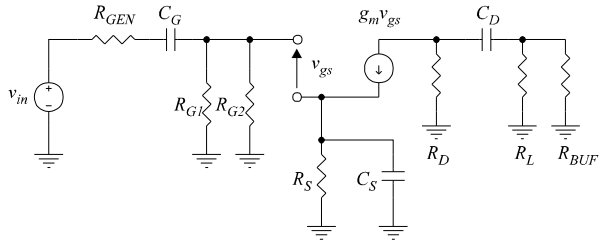
$$t_{H1} = (C_{M1} + C_{GS}) \cdot (R_{in} \parallel R_{GEN}) \quad (13)$$

$$t_{H2} = (C_{M2} + C_{BUF} + C_{DS}) \cdot (R_D \parallel R_L \parallel R_{BUF}) \quad (14)$$

Approximated upper frequency limit can be defined as:

$$f_{H3dB} \approx \frac{1}{2\pi \cdot (t_{H1} + t_{H2})} \quad (15)$$

Low frequency:
The lower cutoff frequency is determined based on the time constant associated with the respective capacitances of the bypass or coupling (calculated time constants for each of the capacity the remaining should be treated asshort circuit). Parasitic capacitances of the MOS transistor are treated as an opening.



Rys. 6. Small signal model of the amplifier of Fig. 2 for the low frequency.

Using the equivalent circuit of Fig. 6 each time constants associated with new capacities can be expressed as follows:

$$t_{L1} = C_G \left(R_{GEN} + R_{G1} \parallel R_{G2}\right) \quad (16)$$

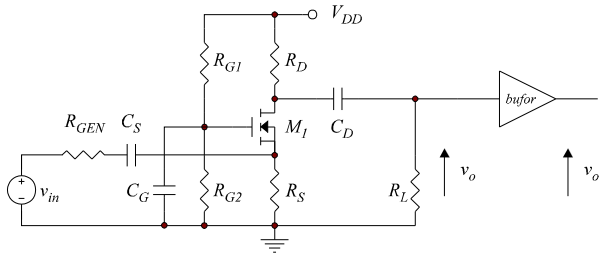
$$t_{L2} = C_S \left(R_S \parallel \frac{1}{g_m} \right) \quad (17)$$

$$t_{L3} = C_D \left(R_D + R_L \parallel R_{BUF}\right) \quad (18)$$

The approximate lower limit frequency can be defined as:

$$f_{L3dB} \approx \frac{1}{2\pi} \left(\frac{1}{t_{L1}} + \frac{1}{t_{L2}} + \frac{1}{t_{L3}} \right) \quad (19)$$

4.2 Common gate circuit (CG):



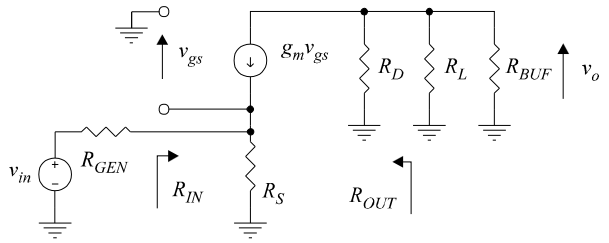
Rys. 7.Diagram of MOS transistor amplifier in the common gate configuration (CG).

4.1.1 Operating point

The operating point is counted identical as for circuit configuration CS.

4.2.2 Small signal analysis

Middle of bandwidth:
Small signal model in the medium frequency range (bandpass) is formed assuming that the coupling capacitance and shunt constitute a short circuit for AC signal, while the parasitic capacitance of the transistor are open circuits.



Rys. 8 Small signal model of the amplifier of Fig. 7 for the midrange frequency.

$$R_{IN} = R_S \parallel \frac{1}{g_m} \quad (20)$$

$$R_{OUT} = R_D \quad (21)$$

$$v_0 = -g_m v_{gs} \left(R_D \parallel R_L \parallel R_{BUF}\right) \quad (22)$$

$$v_{gs} = -\frac{R_{IN}}{R_{IN} + R_{GEN}} v_{in} \quad (23)$$

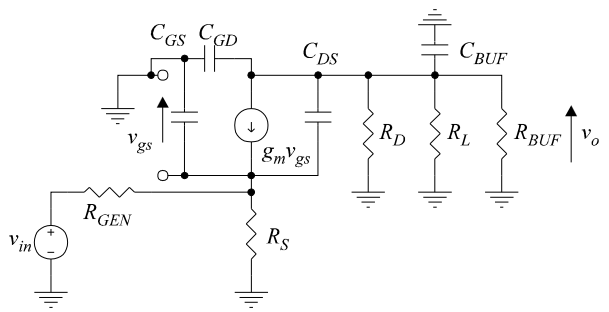
$$\frac{v_0}{v_{in}} = \frac{R_{IN}}{R_{IN} + R_{GEN}} g_m \left(R_D \parallel R_L \parallel R_{BUF}\right) \quad (24)$$

High frequency
The upper cut-off frequency is determined based on the time constants associated with the respective capacities parasitic of the MOS transistor. These constants are counted for the parasitic capacitance on the assumption that the other parasitic capacitances are the opening. Fig. 9 shows that the different time constants are equal to:

$$t_{H1} = C_{GS} \left(R_{GEN} \parallel R_S \parallel \frac{1}{g_m} \right) \quad (25)$$

$$t_{H2} = \left(C_{GD} + C_{BUF}\right) \cdot \left(R_D \parallel R_L \parallel R_{BUF}\right) \quad (26)$$

$$t_{H3} = C_{DS} \left(R_D \parallel R_L \parallel R_{BUF} + \frac{R_D \parallel R_L \parallel R_{BUF} g_m - 1}{\frac{1}{R_{GEN} \parallel R_S} - g_m} \right) \quad (27)$$



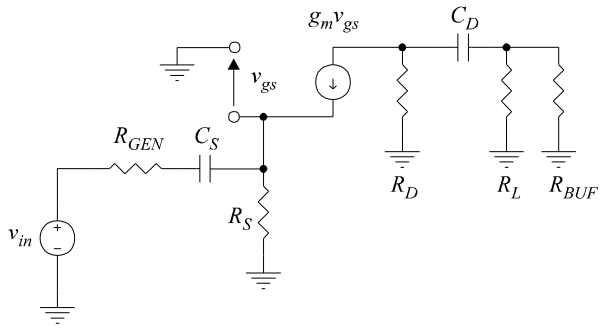
Rys. 9. Small signal model of the amplifier in the CG configuration for the high frequency.

Approximate upper frequency limit can be defined as:

$$f_{H3dB} \approx \frac{1}{2\pi \cdot (t_{H1} + t_{H2} + t_{H3})} \quad (28)$$

Low frequency:
The lower cutoff frequency is determined based on the time constant associated with the respective capacitances of the bypass or coupling (calculated time constants for each of the capacity the remaining should be treated as short circuit). while the parasitic capacitance of the transistor are open circuits.. The time constant associated with the C_G capacitance does not

occur because of not passing the signal from the source to the gate (because of the infinite resistance of the gate).



Rys. 10. Small signal model of the amplifier of Fig. 7 for the low frequency.

From the Fig. 10 the time constants are:

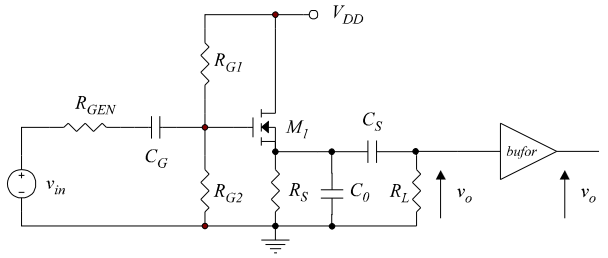
$$t_{L1} = C_S\left(R_{GEN} + R_S \parallel \frac{1}{g_m}\right) \tag{29}$$

$$t_{L2} = C_D\left(R_D + R_L \parallel R_{BUF}\right) \tag{30}$$

The approximate lower limit frequency can be defined as:

$$f_{L3dB} \approx \frac{1}{2\pi}\left(\frac{1}{t_{L1}} + \frac{1}{t_{L2}}\right) \tag{31}$$

4.3 Common drain circuit (CD):



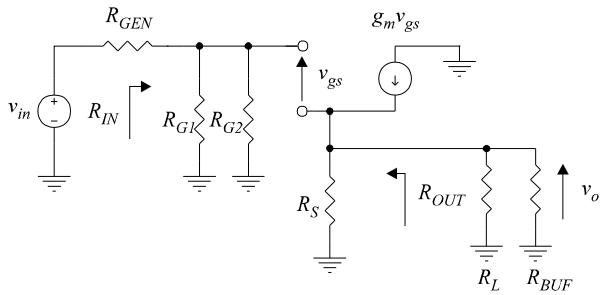
Rys. 11. Diagram of MOS transistor amplifier in the common drain configuration (CD).

4.3.1 Operating point

The operating point is counted identical as for circuit configuration CS. The only difference is that drain voltage is equal to the supply voltage

4.3.2 Small signal analysis:

Middle of bandwidth:
Small signal model in the medium frequency range (bandpass) is formed assuming that the coupling capacitance and shunt constitute a short circuit for AC signal, while the parasitic capacitance of the transistor are open circuits. Additional small capacitance C_0 (35pF) affects high frequency only so in the midrange can be considered as opening.



Rys. 12. Small signal model of the amplifier in CD circuit of Fig. 11 for the midrange frequency.

On the basis of the diagram shown in Fig. 12 each resistances, voltages, and the gain can be determined as follows:

$$R_{IN} = R_{G1} \parallel R_{G2} \tag{32}$$

$$R_{OUT} = R_S \parallel \frac{1}{g_m} \tag{33}$$

$$v_0 = g_m v_{gs}\left(R_S \parallel R_L \parallel R_{BUF}\right) \tag{34}$$

$$v_g = \frac{R_{IN}}{R_{IN} + R_{GEN}} v_{in} \tag{35}$$

$$v_{gs} = v_g - v_s = v_g - v_0 = v_g - g_m v_{gs}\left(R_S \parallel R_L \parallel R_{BUF}\right) \tag{36}$$

$$v_{gs} = v_g \frac{1}{1 + g_m\left(R_S \parallel R_L \parallel R_{BUF}\right)} \tag{37}$$

$$\frac{v_0}{v_{in}} = \frac{R_{IN}}{R_{IN} + R_{GEN}} \frac{g_m\left(R_S \parallel R_L \parallel R_{BUF}\right)}{1 + g_m\left(R_S \parallel R_L \parallel R_{BUF}\right)} \tag{38}$$

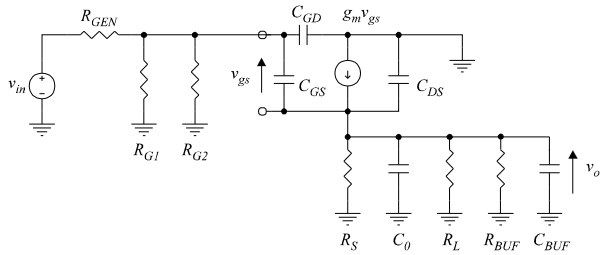
High frequency
The upper cut-off frequency is determined based on the time constants associated with the respective capacities parasitic of the MOS transistor. These constants are counted for the parasitic capacitance on the assumption that the other parasitic capacitances are the opening. Fig. 13 shows that the different time constants are equal to:

$$t_{H1} = C_{GD}\left(R_{GEN} \parallel R_{G1} \parallel R_{G2}\right) \tag{39}$$

$$t_{H2} = \left(C_{DS} + C_0 + C_{BUF}\right) \cdot \left(\frac{1}{g_m} \parallel R_S \parallel R_L \parallel R_{BUF}\right) \tag{40}$$

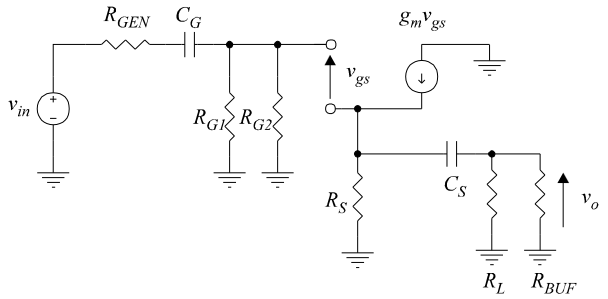
$$t_{H3} = C_{GS}\left(\frac{R_{GEN} \parallel R_{G1} \parallel R_{G2} + R_S \parallel R_L \parallel R_{BUF}}{1 + g_m R_S \parallel R_L \parallel R_{BUF}}\right) \tag{41}$$

$$f_{H3dB} \approx \frac{1}{2\pi \cdot (t_{H1} + t_{H2} + t_{H3})} \tag{42}$$



Rys. 13. Small signal model of the amplifier in CD circuit of Fig. 11 for the high cut-off frequency.

Low frequency:
The lower cutoff frequency is determined based on the time constant associated with the respective capacitances of the bypass or coupling (calculated time constants for each of the capacity the remaining should be treated as short circuit). while the parasitic capacitance of the transistor. and small capacity of C_0 are open circuit.



Rys. 14. ZSmall signal model of the amplifier in CD circuit of Fig. 11 for the low frequency.

From the Fig. 40 the time constants are:

$$t_{L1} = C_G\left(R_{GEN} + R_{G1} \parallel R_{G2}\right) \tag{43}$$

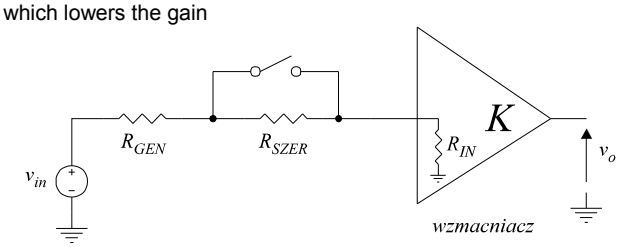
$$t_{L2} = C_S\left(\frac{1}{g_m} \parallel R_S + R_L \parallel R_{BUF}\right) \tag{44}$$

Approximate lower frequency limit can be defined as:

$$f_{L3dB} \approx \frac{1}{2\pi}\left(\frac{1}{t_{L1}} + \frac{1}{t_{L2}}\right) \tag{45}$$

4.4 Measurement of the input resistance of the amplifiers

Input resistance is measured using additional resistor R_{SZER} connected in series with the internal generator resistance R_{GEN}. During normal operation, it is shorted by the switch located on the frontpanel. After pressing the button marked R_{IN} there is an opening, causing the connection in series of resistor R_{SZER}, which lowers the gain



Rys. 15. The measurement method of the input resistance of the amplifier

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Marking the output voltage with closed and opened resistor R_{SZER} as v_0 and $v_0^{'}$ respectively:

$$v_o = K \cdot \frac{R_{IN}}{R_{IN} + R_{GEN}} \cdot v_{in} \tag{46}$$

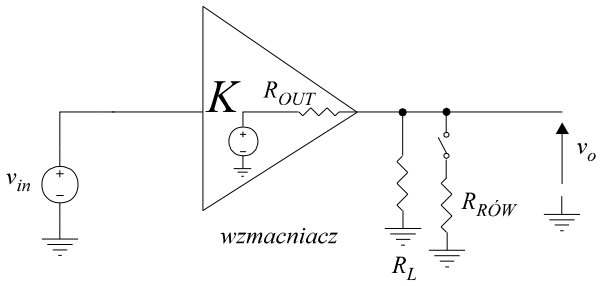
$$v_o^{'} = K \cdot \frac{R_{IN}}{R_{IN} + R_{GEN} + R_{SZER}} \cdot v_{in} \tag{47}$$

$$\frac{v_o}{v_o^{'}} = \frac{R_{IN} + R_{GEN} + R_{SZER}}{R_{IN} + R_{GEN}} \tag{48}$$

$$R_{IN} = \frac{v_o^{'}}{v_o - v_o^{'}} \cdot R_{SZER} - R_{GEN} \tag{49}$$

4.5 Measurement of the input resistance of the amplifiers

Input resistance is measured using additional resistor $R_{RÓW}$ connected in parallel with the amplifier load resistance R_L. During normal operation the $R_{RÓW}$ resistor is disconnected. In the order of resistance measuring it is connected by the switch R_{OUT}.



Rys. 16. The measurement method of the output resistance of the amplifier

Marking the output voltage with disconnected and connected resistor $R_{RÓW}$ as v_0 and $v_0^{'}$, respectively:

$$v_o = K \cdot \frac{R_L}{R_L + R_{OUT}} \cdot v_{in} \tag{50}$$

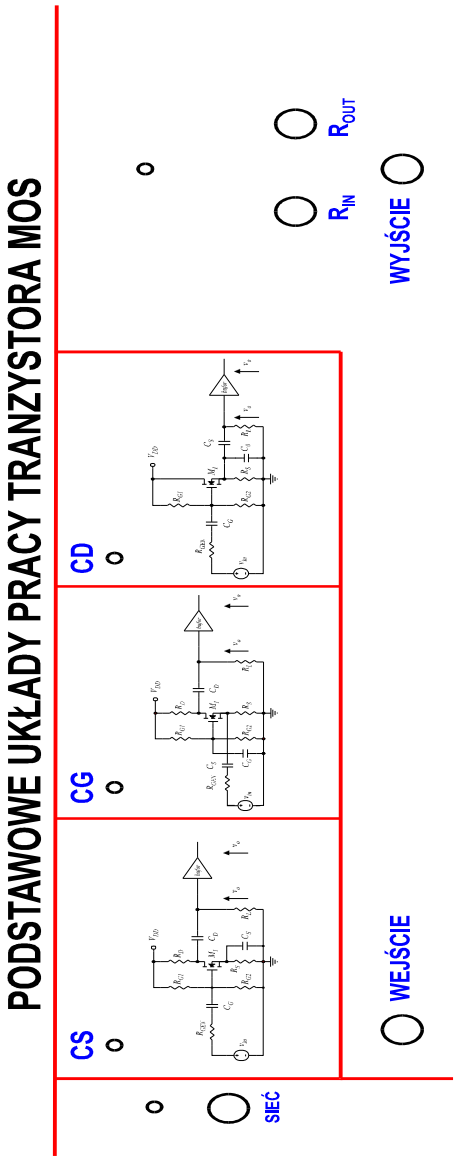
$$v_o^{'} = K \cdot \frac{R_L \parallel R_{RÓW}}{R_L \parallel R_{RÓW} + R_{OUT}} \cdot v_{in} \tag{51}$$

$$\frac{v_o}{v_o^{'}} = \frac{R_L \parallel R_{RÓW} + R_{OUT}}{R_L \parallel R_{RÓW}} \frac{R_L}{R_L + R_{OUT}} \tag{52}$$

$$R_{OUT} = \frac{R_L\left(1 - \frac{v_0}{v_0^{'}}\right)}{\frac{v_0}{v_0^{'}} - \frac{R_L}{R_L \parallel R_{RÓW}}} \tag{53}$$

4.6 Parameters data of transistor in various circuits

Parameter	Unit	CS	CG	CD
K_N	μA/V^2	312,32	323,46	309,15
V_T	V	1,272	1,264	1,252
C_{DS}	pF	12,34	12,36	11,42
C_{GS}	pF	9,33	9,74	8,99
C_{GD}	pF	1,7	1,84	1,93
R_{GEN}	Ω	50	50	50
R_{BUF}	MΩ	1	1	1
C_{BUF}	pF	3	3	3
C_0	pF	nie ma	nie ma	35
R_{SZER}	kΩ	300,8	2,87	306,5
$R_{RÓW}$	kΩ	21,8	20,49	3,142
C_G	nF	9,15	9,20	9,17
C_S	μF	0,98	0,98	1,001
C_D	nF	100	100	100
R_{G1}	kΩ	752,8	755,5	754,5
R_{G2}	kΩ	479	481,3	480,6
R_S	kΩ	21,97	22,26	22,31
R_D	kΩ	46,68	46,83	nie ma
R_L	kΩ	46,8	46,78	13,35
V_{DD}	V	12	12	12



Rys. 17. The front panel of the laboratory circuit.

Literatura:

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[2] A. Guziński, „Liniowe elektroniczne układy analogowe”, WNT, Warszawa 1992.

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