Continuous - Time Integrated Filter – laboratory

Laboratory organization

During the laboratory, each student should perform five exercises using the PSPICE simulator and the simulation results should be sent to the laboratory operator at his email address. Each exercise is scored equally (20 points) and the final grade from the laboratory is determined on the basis of the following criterion:

Mark	Points from:	Points to:
2	0	50
3	51	60
3,5	61	70
4	71	80
4,5	81	90
5	91	100

The simulation results should be placed in a table, the pattern of which is attached to each exercise and also in the zipped form is available here: http://www.ue.eti.pg.gda.pl/~bpa/fscc/lab_tables.zip. As models of MOS transistors, models for AMI C5 technology available here: http://www.ue.eti.pg.gda.pl/~bpa/fscc/ami_c5.lib should be used.

Tasks to be performed during the laboratory

Exercise 1: PSPICE simulation of Operational Transconductance Amplifier (OTA)

The schematic diagram of the tested amplifier is shown in the figure below, while the dimensions of MOS transistors are given in Table 1. Dimension description 4 * 2/5 means 4 MOS transistors, each with dimensions of 2/5 (W/L) connected in parallel. To enter several elements connected in parallel, you can use:

- manual, multiple entries of devices with unique names connected to the same nodes or
- one entry of the MOS device with an additional parameter M = x, where x is the number of parallel connected identical MOS transistors.

It is obligatory to use the names of nodes given in italics in green on the amplifier drawing when creating the connection list. The substrates of nMOS and pMOS transistors should be connected to Vss or Vdd, respectively. Two independent voltage sources must be connected to the input of the amplifier:

- **Vid** setting only the value of the differential voltage applied to the input of the amplifier, and
- **Vcm** setting only the value of the input common voltage.

Values of supply voltages and polarizing current are given in Table 2.

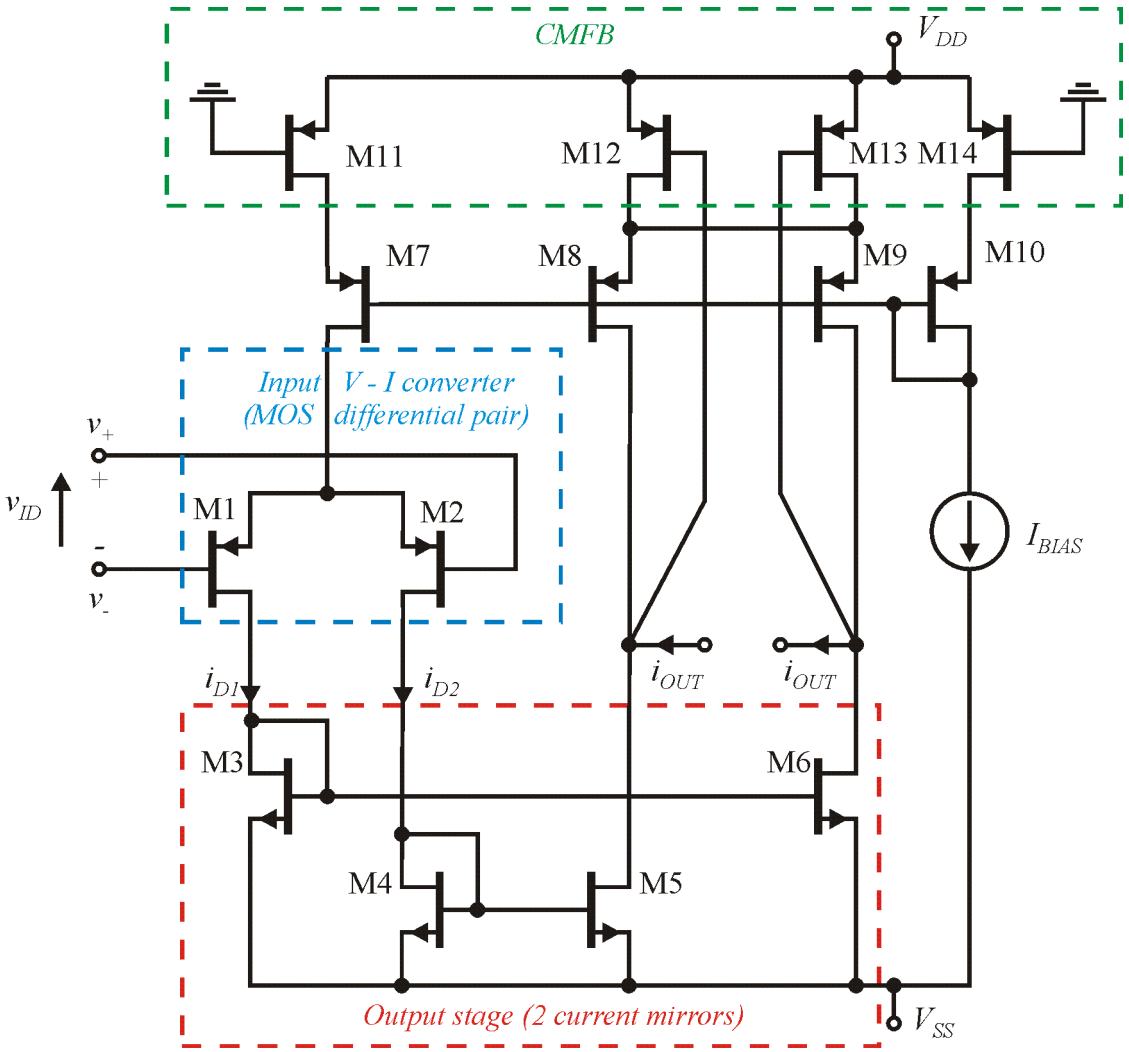

Fig. 1. Diagram of the tested OTA. At each node there are obligatory names to use when preparing the netlist (green).

Table 1. Dimensions of MOS devices of the tested OTA amplifier.

Device	**Dimensions W/L [µm/µm]**
M1, M2	12/4
M3, M4	2/2
M5, M6	4 * 2/2
M7	2 * 4/2
M8, M9	4 * 4/2
M10	4/2
M11	2 * 2/2
M12, M13	4 * 2/2
M14	2/2

Tabela 2. Napięcia i prądy zasilające.

Parametr	**Wartość**
Vdd	2,5V
Vss	-2,5V
Ibias	10µA

Please follow the instructions below and record results in the table presented in appendix:
1) Enter the connection list of the tested amplifier, add the input voltage source, voltage supply and bias current.

2) As a load, the voltage source of 0 volts should be connected between the ***out_p*** and ***out_m*** nodes. It creates ideal short circuit and additionally its current can be observed. For such a configuration and zero input voltage values, DC analysis should be carried out to find operating point (.OP) and the currents of the individual transistors should be recorded and the voltage value on the output should be saved. Compare the saved currents with the reference values and if you find the differences, you should find the error in the connection list and correct it.
The reference values of drain currents:

NAME	M1	M2	M3	M4	M5
MODEL	pfet	pfet	nfet	nfet	nfet
ID	-9.76E-06	-9.76E-06	9.76E-06	9.76E-06	4.00E-05
NAME	M6	M7	M8	M9	M10
MODEL	nfet	pfet	pfet	pfet	pfet
ID	4.00E-05	-1.95E-05	-4.00E-05	-4.00E-05	-1.00E-05
NAME	M11	M12	M13	M14	
MODEL	pfet	pfet	pfet	pfet	
ID	-1.95E-05	-4.00E-05	-4.00E-05	-1.00E-05	

3) When loaded as in point 2) DC analysis should be performed with the differential input voltage ***Vid*** change in the range from -1V to 1V. Please find the value of amplifier transconductance parameter (read as output current in respect to ***Vid*** derivative), input voltage ***Vid*** for which 1% current error occurs and ***Vid*** voltage for which a 1% transconductance error occurs.
4) From the simulation as in point 3) read off the range of DC voltages seen at the amplifier output as ***Vid*** changes from -1V to 1V.
5) For still the same load, a time analysis should be performed with harmonic stimulation of frequency 10kHz and at different amplitudes of the input voltage. Find the amplitude of the input harmonic voltage for which output current exhibits 1% THD. This amplitude should be determined with an accuracy of 10mV.
6) For the same load, frequency analysis should be performed and the frequency of the 3dB drop in output current magnitude should be found. Similarly please find frequency for which 1° output current phase change occurs (in respect to low frequencies).
7) Remove the load in the form of a voltage source and perform the AC analysis to find voltage gain. On this basis, please determine the voltage gain for low frequencies and the frequency for which the voltage gain drops by 3dB.
8) The amplifier should be loaded with a noiseless resistor of value 1Ω and then a noise analysis should be performed. Please find the input referred RMS value of the noise integrated in the frequency rage from 10Hz to 10MHz.
9) Determine the dynamic range (DR) of the amplifier as the ratio of RMS values determined in point 5 and point 8.
10) The values of the differential input and output capacitances should be determined. These capacitances can be determined by definition, by measuring the voltage and current of an independent source connected respectively to the input or output of the OTA and then determining the capacitance value by transforming the dependence on the capacitor impedance.

$$C = \frac{1}{2\pi f Z_C} = \frac{I_{of\_the\_source}}{2\pi f V_{of\_the\_source}}$$

The above formula is valid only in the scope of the capacitive nature of the input/output impedance, i.e. for frequencies for which the phase shift between voltage and current of this source is equal to 90°.

Appendix - protocol pattern. This table should be copied, completed and then sent to the teacher's email address.

Exercise 1: PSPICE simulation of Operational Transconductance Amplifier			
No	**Description**	**Unit**	**Value**
1	Name of the student		
2	Date		
3	Simulation according to the point 2 – value of output voltage	mV	
4	Simulation according to the point 3 – transconductance @ V_{ID} =0V	μS	
5	Simulation according to the point 3 – V_{ID} range of 1% output current error	mV	
6	Simulation according to the point 3 – V_{ID} range of 1% transconductance error	mV	
7	Simulation according to the point 4 – range of output voltages	mV	
8	Simulation according to the point 5 – amplitude of V_{ID} for 1% THD at output current	mV	
9	Simulation according to the point 6 – 3dB frequency	MHz	
10	Simulation according to the point 6 – frequency of 1° phase change	MHz	
11	Simulation according to the point 7 – voltage gain for low frequencies	dB	
12	Simulation according to the point 7 – frequency of 3dB voltage passbad	kHz	
13	Simulation according to the point 8 – input referred RMS noise integrated in 10Hz-10MHz band	mV	
14	Simulation according to the point 9 - DR	dB	
15	Simulation according to the point 10 - input differential capacitance C_{ID}	fF	
16	Simulation according to the point 10 - output differential capacitance C_{OD}	fF	
17	Here you can put your own comments and conclusions from the exercise.		

Exercise 2: PSPICE simulation of the positive, second generation current conveyor (CCII+).

The schematic diagram of the tested CCII + current conveyor is shown in Figure 2. It is obligatory to use the names of nodes given in italics in green when creating the netlist. The substrates of nMOS and pMOS transistors should be connected to ***Vss*** or ***Vdd***, respectively. A separate voltage source ***Vy*** should be connected to the ***Y*** input of the amplifier. Values of supply voltages and polarizing currents are given in Table 3.

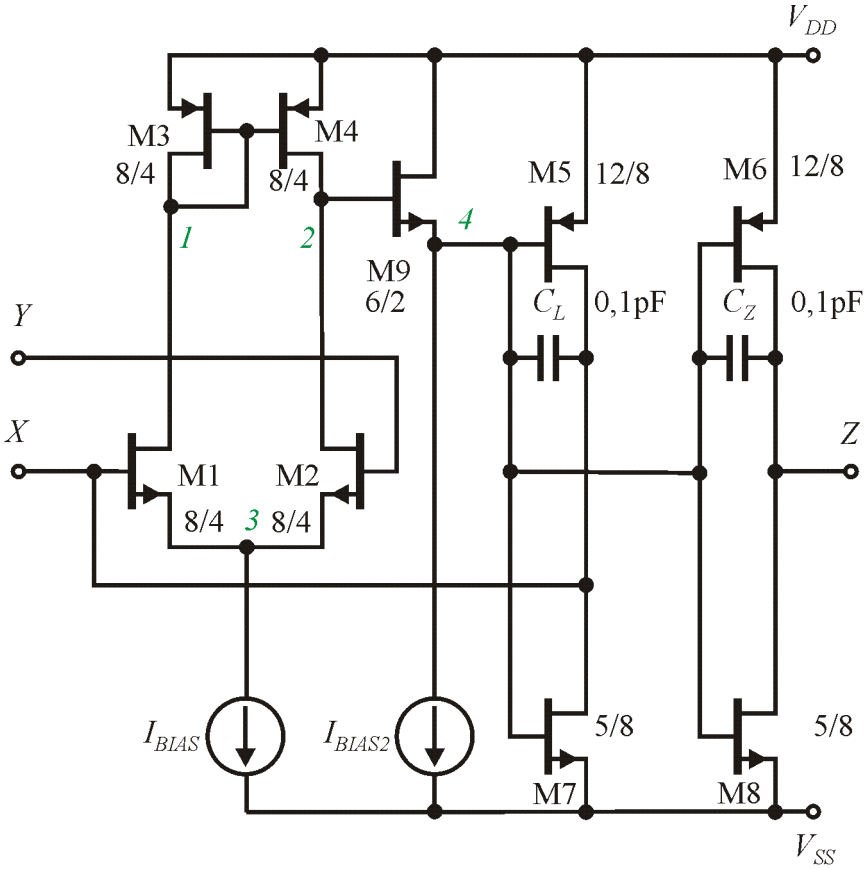

Fig. 2. Diagram of the tested CCII+ current conveyor. Obligatory names of the nodes in netlist are given in green italic. The transistor dimensions are given in μm.

Tabele 3. Supply voltages and currents.

Parameter	**Value**
Vdd	2,5V
Vss	-2,5V
Ibias, Ibias2	10μA

Please follow the instructions below and record results in the table presented in appendix:

1) Enter the connection list of the tested amplifier, the ***Vy*** input voltage source and the supply voltages and currents.
2) As a load, a 10kΩ resistor must be connected between nodes ***X*** and ***0*** and a zero value voltage source between ***Z*** node and ***0***. For such configuration and zero input voltage ***Vy***, DC analysis should be performed, the currents of individual transistors should be recorded as well as the voltage on the output ***X*** and current on output ***Z*** should be compared. In the case of differences, the error in the connection list should be found and corrected.

The reference values of drain currents:

NAME	M1	M2	M3	M4	M5
MODEL	nfet	nfet	pfet	pfet	pfet
ID	5.00E-06	5.00E-06	-5.00E-06	-5.00E-06	-5.88E-05
NAME	M7	M6	M8	M9	
MODEL	nfet	pfet	nfet	nfet	
ID	5.87E-05	-5.88E-05	5.87E-05	1.00E-05	

3) When connecting the conveyor as in point 2) DC should be performed with the input voltage ***Vy*** changes in the range from -1V to 1V. Provide the following values from the analysis: voltage amplification from ***Vy*** to ***Vx*** @ ***Vy*** = 0, transconductance gain from ***Vy*** to voltage source ***Vz***@***Vy***=0, and range of input voltages for which above mentioned gains do not differ by more than 1% in relation to the theoretical values.
4) When connecting the conveyor as in point 2) please perform frequency analysis and find the 3dB passband at voltage output ***Vx*** and current source ***Vz***. You should also find the frequency of the 1° phase change of the output signal.
5) Disconnect the ***Vz*** load source and perform frequency simulation. Please read the voltage gain to the ***Z*** output and the frequency of the pole of the ***Z*** node (frequency of the voltage drop by 3dB).
6) Please perform simulations necessary to determine the resistance of node ***X*** (without resistor ***Rx***) and resistance of the node ***Z***.

Appendix - protocol pattern. This table should be copied, completed and then sent to the teacher's email address.

Exercise 2: PSPICE simulation of the CCII+			
No	**Description**	**Unit**	**Value**
1	Name of the student		
2	Date		
3	Simulation according to the point 2 – value of **Vx** voltage	mV	
4	Simulation according to the point 2 – current of the voltage source **Vz**	nA	
5	Simulation according to the point 3 – gain to **Vx** node	V/V	
6	Simulation according to the point Symulacja wg pkt. 3 – transkonduktancja do **I(Vz)**	μS	
7	Simulation according to the point 3 - range of voltages at **Vy** with voltage **Vx** gain error smaller than 1%	mV	
8	Simulation according to the point 3 – range of voltages at **Vy** with transconductance of **I(Vz)** error smaller than 1%.	mV	
9	Simulation according to the point 4 – frequency of 3dB voltage **Vx** passband	MHz	
10	Simulation according to the point 4 – frequency of 3dB current **I(Vz)** passband	MHz	
11	Simulation according to the point 4 – frequency of 1° voltage **Vx** phase change	MHz	
12	Simulation according to the point 4 – frequency of 1° current **I(Vz)** phase change	MHz	
13	Simulation according to the point 5 – voltage gain on non loaded **Z** node	dB	
14	Simulation according to the point 5 – frequency of the non loaded 3dB passband at node **Z**	kHz	
15	Simulation according to the point 6 – resistance of the **X** node	Ω	

16	Simulation according to the point 6 – resistance of the **Z** node	kΩ	
17	Here you can put your own comments and conclusions from the exercise.		

Exercise 3: Investigation of the VI-order, lowpass, cascade, OTA-C filter.

Before starting the exercise, first please design the subject of investigation: lowpass, VI-order filter using Butterworth approximation and cascade method. The filter should be fully differential, OTA-C using OTA amplifiers from exercise no 1. Desired parameters of the filter: ***H***=1, ***fo***=500kHz. During design, the actual capacitance values should be reduced by the sum of the input and output capacitances of the OTA amplifiers occurring in the given signal nodes. The amplifiers from exercise 1 should be embedded as subcircuits in the whole filter design. Simultaneously, simulations of the ideal filter should be performed (e.g. by plotting the ideal transmittance characteristics with the LAPLACE command or by simulating the ideal RLC prototype, denormalized to the frequency of 500 kHz).

Please follow the instructions below and record results in the table presented in appendix:

1) Perform a frequency simulation and plot the amplitude and phase responses. Determine the 3dB frequency of the filter and the frequency for which the output phase is equal to -270 °.
2) Simultaneously execute a simulation for the ideal filter. Find the frequency for which the amplitude response of the real filter differs by more than 1dB compared to the ideal filter. Similarly, a frequency should be found for which the phase response of the real filter differs by more than 1° compared to the ideal filter.
3) Please perform transient analysis with harmonic signal at input of 10kHz frequency and different amplitudes. Find the amplitude of the input harmonic signal for which the THD distortion of the output voltage is 1%. This amplitude should be determined with an accuracy of 10mV.
4) The noise analysis should be performed and the RMS value of input referred noise integrated in band from 10Hz to 1MHz should be calculated.
5) Determine the dynamic range (DR) of the amplifier as the ratio of RMS values determined in point 3 and point 4.
6) Perform a operating point analysis and read the filter's power consumption from the output file.

Appendix - protocol pattern. This table should be copied, completed and then sent to the teacher's email address.

Exercise 3: Investigation of the VI-order, lowpass, cascade, OTA-C filter.			
No	**Description**	**Unit**	**Value**
1	Name of the student		
2	Date		
3	Here please insert designed filter schematic including capacitor's values.		
4	Simulation according to the point 1 – 3dB frequency of the filter	kHz	
5	Simulation according to the point 1 – frequency of -270° phase at output	kHz	
6	Simulation according to the point 2 – frequency of 1dB error of amplitude response	kHz	
7	Simulation according to the point 2 – frequency of 1° error of phase response	kHz	
8	Simulation according to the point 3 – amplitude of V_{ID} for 1% THD at output	mV	
9	Simulation according to the point 4 – input referred RMS value of noise integrated in band from 10Hz to 10MHz	μV	
10	DR Simulation according to the point 5	dB	

11	Simulation according to the point 6 – power consumption	mW	
12	Here you can put your own comments and conclusions from the exercise.		

Exercise 4: Investigation of the VI-order, bandpass, OTA-C filter.

Before starting the exercise, first please design the subject of investigation: bandpass, VI-order filter using Butterworth approximation and direct simulation of the RLC ladder prototype. The filter should be fully differential, OTA-C using OTA amplifiers from exercise no 1. Desired parameters of the filter: ***H***=1, ***fo***=400kHz, passband=100kHz. During design, the actual capacitance values should be reduced by the sum of the input and output capacitances of the OTA amplifiers occurring in the given signal nodes. The amplifiers from exercise 1 should be embedded as subcircuits in the whole filter design. Simultaneously, simulations of the ideal filter should be performed (e.g. by plotting the ideal transmittance characteristics with the LAPLACE command or by simulating the ideal RLC prototype, denormalized to the frequency of 400 kHz).

Please follow the instructions below and record results in the table presented in appendix:

1) Perform a frequency simulation and plot the amplitude and phase responses. Determine the filter 3dB frequency (in relation to the level for the center frequency), and the center frequency by determining the frequency for which the output phase is equal to 0 °.
2) Simultaneously execute a simulation of the ideal filter. The ideal and real characteristics should be compared. What is the gain for the ideal filter and for the real filter for f = 400kHz? Where do the large differences in amplitude characteristics for the center of the filter band come from?
3) The transient should be performed with harmonic excitation at 400 kHz frequency and at different amplitudes of the input voltage. Find the amplitude of the input harmonic voltage for which the distortion THD of the output voltage is 1%. This amplitude should be determined with an accuracy of 10mV. Why is this amplitude greater than for a single OTA amplifier?
4) The noise analysis should be performed and the input referred RMS noise integrated in the band from 300kHz to 500kHz value should be found.
5) Determine the dynamic range (DR) of the amplifier as the ratio of RMS values determined in point 3 and point 4.
6) Perform a operating analysis and read the filter's power consumption from the output file.

Appendix - protocol pattern. This table should be copied, completed and then sent to the teacher's email address.

Exercise 4: Investigation of the VI-order, bandpass, OTA-C filter.			
No	**Description**	**Unit**	**Value**
1	Name of the student		
2	Date		
3	Here please insert designed filter schematic including capacitor's values.		
4	Simulation according to the point 1 – center and 3dB frequencies of the designed filter	kHz	
5	Simulation according to the point 2 – center and 3dB frequencies of the ideal filter	kHz	
6	Simulation according to the point 2 – gain error for f=400kHz	dB	
7	Simulation according to the point 3 – amplitude of V_{ID} for 1% THD at output	mV	
8	Simulation according to the point 4 – input referred RMS noise integrated in band from 300kHz to 500kHz	μV	
9	DR according to the point 5	dB	
10	Simulation according to the point 6 – power dissipation	mW	

11	Here you can put your own comments and conclusions from the exercise and answers to questions from point 2 and 3.

Exercise 5: Comparative investigation of the VI-order, lowpass, OTA-C filters designed using cascade and RLC ladder prototype simulation methods.

Before starting the exercise, first please design the subject of investigation: lowpass, VI-order filter with Butterworth approximation using RLC ladder prototype simulation method. The filter should be fully differential, OTA-C using OTA amplifiers from exercise no 1. Desired parameters of the filter: $\boldsymbol{H}$=1, $\boldsymbol{fo}$=500kHz. During design, the actual capacitance values should be reduced by the sum of the input and output capacitances of the OTA amplifiers occurring in the given signal nodes. The filter parameters are identical as in exercise 3, the only difference is the design method. Simultaneously, simulations of the ideal filter should be performed (e.g. by plotting the ideal transmittance characteristics with the LAPLACE command or by simulating the ideal RLC prototype, denormalized to the frequency of 500 kHz).

Please follow the instructions below and record results in the table presented in appendix:

1) Execute a frequency simulation and plot the amplitude and phase responses. Determine the 3dB frequency of the filter and the frequency for which the output phase is equal to -270°.
2) Simultaneously execute a simulation of the ideal filter. Find the frequency for which the amplitude response of the real filter differs by more than 1dB compared to the ideal filter. Similarly, a frequency should be found for which the phase response of the real filter differs by more than 1° compared to the ideal filter.
3) The transient analysis should be performed with harmonic stimulation of 10 kHz frequency and at different amplitudes of the input voltage. Find the amplitude of the input harmonic voltage for which the distortion THD of the output voltage is 1%. This amplitude should be determined with an accuracy of 5mV.
4) The noise analysis should be performed and the RMS value of input referred noise integrated in band from 10Hz to 1MHz should be calculated.
5) Determine the dynamic range (DR) of the amplifier as the ratio of RMS values determined in point 3 and point 4.
6) Perform a operating point analysis and read the filter's power consumption from the output file.
7) Execute the Monte Carlo frequency analysis with changes of the threshold voltage and K coefficients of transistors in the 1% range, 100 runs of this analysis should be performed. This analysis should be performed both for the filter from exercises 3 and 5. On the basis of this analysis, one should find the range of changes of the gain value for low frequencies as well as the range of frequency changes for which the phase is equal to -270 °.

Appendix - protocol pattern. This table should be copied, completed and then sent to the teacher's email address.

Exercise 5: Comparative investigation of the VI-order, lowpass, OTA-C filters designed using cascade and RLC ladder prototype simulation methods.				
No	**Description**	**Unit**	**Filtr z ćw. 3**	**Filtr z ćw. 5**
1	Name of the student			
2	Date			
3	Here please insert designed filter schematic including capacitor's values.			
4	Simulation according to the point 1 – 3dB frequency of the filter	kHz		
5	Simulation according to the point 1 – frequency of -270° phase at output	kHz		

6	Simulation according to the point 2 – frequency of 1dB error of amplitude response	kHz		
7	Simulation according to the point 2 – frequency of 1° error of phase response	kHz		
8	Simulation according to the point 3 – amplitude of V_{ID} for 1% THD at output	mV		
9	Simulation according to the point 4 – input referred RMS noise integrated in band from 10Hz to 1MHz	μV		
10	DR according to the point 5	dB		
11	Simulation according to the point 6 – power dissipation	mW		
12	Simulation according to the point 7 – range of filter gain	dB		
13	Simulation according to the point 7 – range of filter center frequency measured for –270° voltage phase at output	kHz		
14	Here you can put your own comments and conclusions from the exercise.			