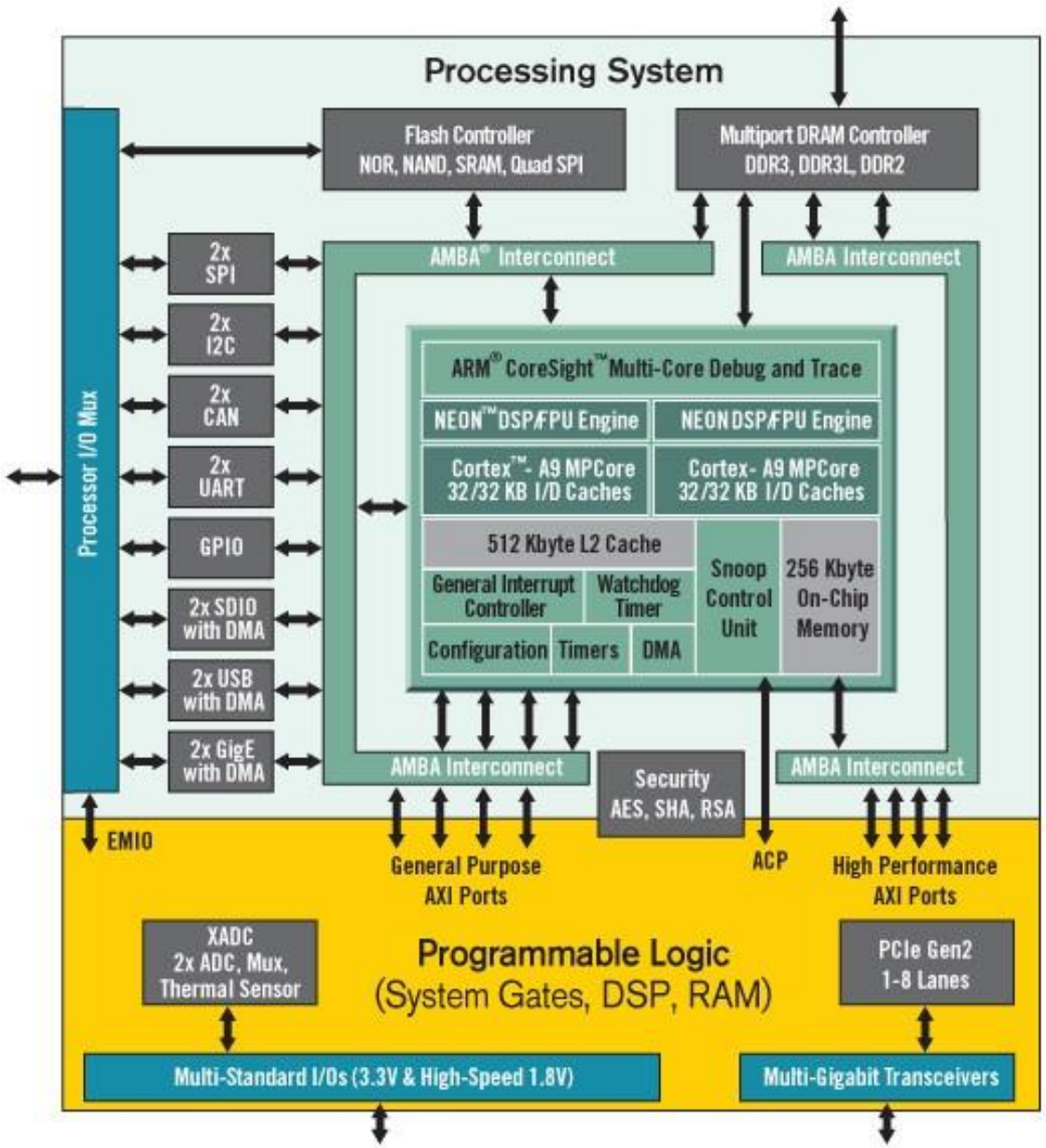
Programowalne Układy System On Chip

XILINX ZYNQ - 7000

Architektura



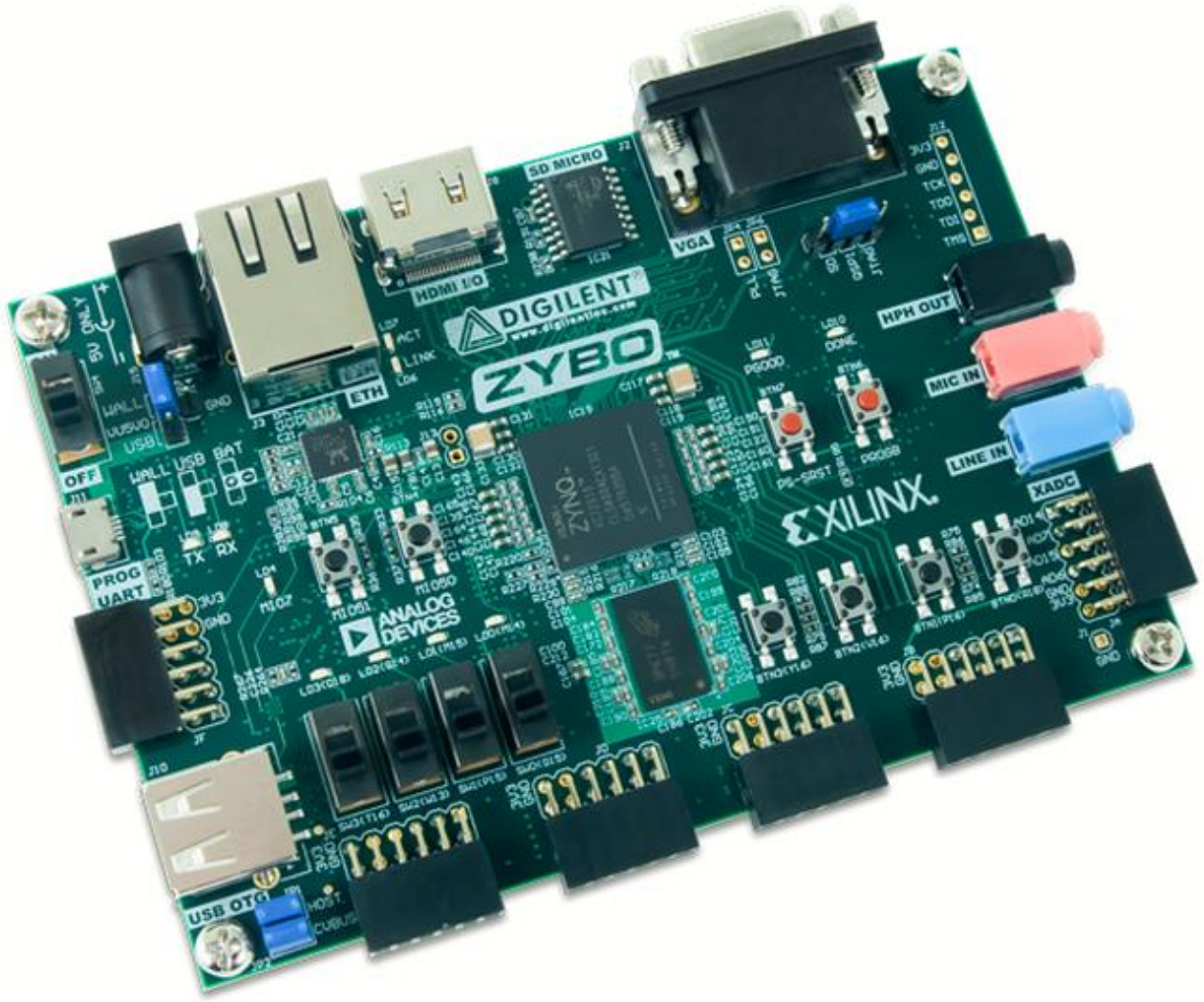
Product table

Zynq®-7000 All Programmable SoCs

XILINX

		Zynq-7000 All Programmable SoC																
		Low-End Portfolio			Mid-Range Devices													
	Device Name	Z-7010	Z-7015	Z-7020	Z-7030			Z-7035			Z-7045			Z-7100				
	Part Number	XC7Z010	XC7Z015	XC7Z020	XC7Z030			XC7Z035			XC7Z045			XC7Z100				
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™																
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor																
	Maximum Frequency	866 MHz			Up to 1 GHz [1]													
	L1 Cache	32 KB Instruction, 32 KB Data per processor																
	L2 Cache	512 KB																
	On-Chip Memory	256 KB																
	External Memory Support [2]	DDR3, DDR3L, DDR2, LPDDR2																
	External Static Memory Support [2]	2x Quad-SPI, NAND, NOR																
	DMA Channels	8 (4 dedicated to Programmable Logic)																
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO																
	Peripherals w/ built-in DMA[2]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO																
	Security[3]	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot																
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts																
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Kintex®-7 FPGA			Kintex-7 FPGA			Kintex-7 FPGA			Kintex-7 FPGA				
	Programmable Logic Cells (Approximate ASIC Gates[4])	28K Logic Cells (~430K)	74K Logic Cells (~1.1M)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)			275K Logic Cells (~4.1M)			350K Logic Cells (~5.2M)			444K Logic Cells (~6.6M)				
	Look-Up Tables (LUTs)	17,600	46,200	53,200	78,600			171,900			218,600			277,400				
	Flip-Flops	35,200	92,400	106,400	157,200			343,800			437,200			554,800				
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)	380 KB (95)	560 KB (140)	1,060 KB (265)			2,000 KB (500)			2,180 KB (545)			3,020 KB (755)				
	Programmable DSP Slices (18x25 MACCs)	80	160	220	400			900			900			2,020				
	Peak DSP Performance (Symmetric FIR)	100 GMACs	200 GMACS	276 GMACs	593 GMACs			1,334 GMACs			1,334 GMACs			2,622 GMACs				
	PCI Express® (Root Complex or Endpoint)	—	Gen2 x4	—	Gen2 x4			Gen2 x8			Gen2 x8			Gen2 x8				
	Analog Mixed Signal (AMS) / XADC[2]	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs																
	Security[3]	AES and SHA 256b Decryption and Authentication for Secure Programmable Logic Configuration																
Speed Grades	Commercial (0C to 85C)	-1			-1									NA				
	Extended (0C to 100C)	-2, -3			-2, -3									N/A				
	Industrial (–40C to 100C)	-1, -1L, -2			-1, -2, -2L													
Packages	Package Type[5]	CLG225[1]	CLG400	CLG485[7]	CLG400	CLG484	SBG485[7]	FBG484	FBG676	FFG676	FBG676	FFG676	FFG900	FBG676	FFG676	FFG900	FFG900	FFG1156
	Size (mm)	13x13	17x17	19x19	17x17	19x19	19x19	23x23	27x27	27x27	27x27	27x27	31x31	27x27	27x27	31x31	31x31	35x35
	Pitch (mm)	0.8	0.8	0.8	0.8	0.8	0.8	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
	Processing System User I/Os (excludes DDR dedicated I/Os)[6]	32	54	54	54	54	54	54	54	54	54	54	54	54	54	54	54	54
	Multi-Standards and Multi-Voltage SelectIO™ Interfaces (1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V)	54	100	150	125	200	50	100	100	100	100	100	212	100	100	212	212	250
	Multi-Standards and Multi-Voltage High Performance SelectIO Interfaces (1.2V, 1.35V, 1.5V, 1.8V)	—	—	—	—	—	100	63	150	150	150	150	150	150	150	150	150	150
	Serial Transceivers	—	—	4	—	—	4	4	4	4	8	8	16	8	8	16	16	16
	Maximum Transceiver Speed (Speed Grade Dependent)	N/A	N/A	6.25 Gb/s	N/A	N/A	6.6 Gb/s	6.6 Gb/s	6.6 Gb/s	12.5 Gb/s	6.6 Gb/s	12.5 Gb/s	12.5 Gb/s	6.6 Gb/s	12.5 Gb/s	12.5 Gb/s	10.3125 Gb/s	10.3125 Gb/s

ZYBO BOARD



- ZYNQ XC7Z010-1CLG400C
- 512MB x32 DDR3 w/ 1050Mbps bandwidth
- Dual-role (Source/Sink) HDMI port
- Artix-7 FPGA:
  - 28K logic cells
  - 240KB Block RAM
  - 80 DSP slices
  - On-chip dual channel, 12-bit, 1 MSPS analog-to-digital converter (XADC)

Karta SD – struktura / Środowisko potrzebne do kompilacji

- ZYBO_BOOT
  - uImage – plik który bootuje cały system.
  - Devicetree.dtb – plik zawierający konfigurację wszystkich urządzeń peryferyjnych.
  - BOOT.bin – kontener zawierający pliki budujące system: u-boot.elf, FSBL.elf, system.bit.
- ROOT_FS – zawiera pliki Linuxa Linaro (533MB) oraz jest dyskiem roboczym systemu operacyjnego 5, link: https://releases.linaro.org/12.09/ubuntu/precise-images/ubuntu-desktop

- ✓ CentOS 6.5
- ✓ Xilinx Vivado – wersja 2014.1+

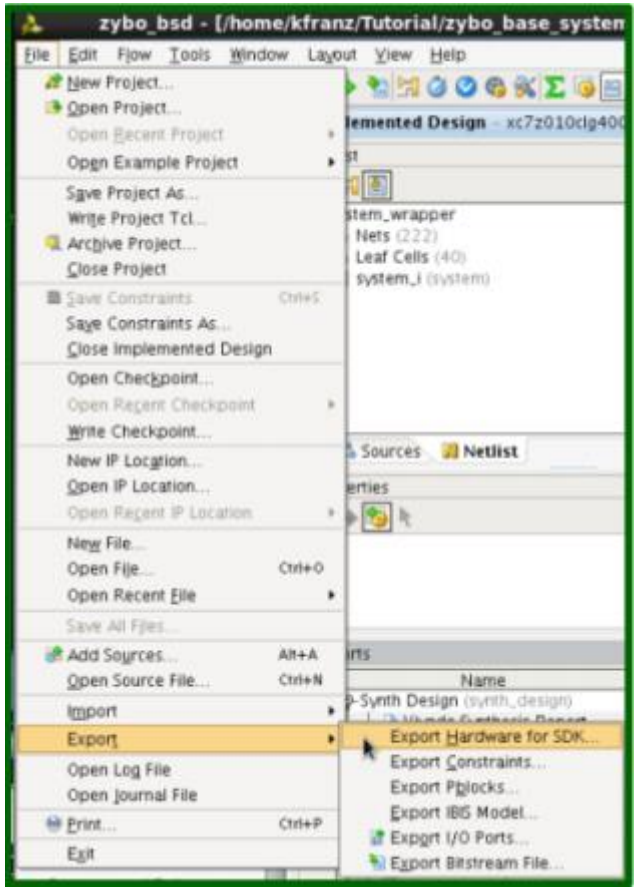
Tworzenie u-boot.elf

Komendy do wpisania w terminal:

- source /opt/Xilinx/Vivado/2014.1/settings64.sh
- git clone git://git.linaro.org/boot/u-boot-linaro-stable.git
- cd u-boot-linaro-stable
- make CROSS_COMPILE=arm-xilinx-linux-gnueabi-zynq_zybo_config
- make CROSS_COMPILE=arm-xilinx-linux-gnueabi
- cp u-boot u-boot.elf

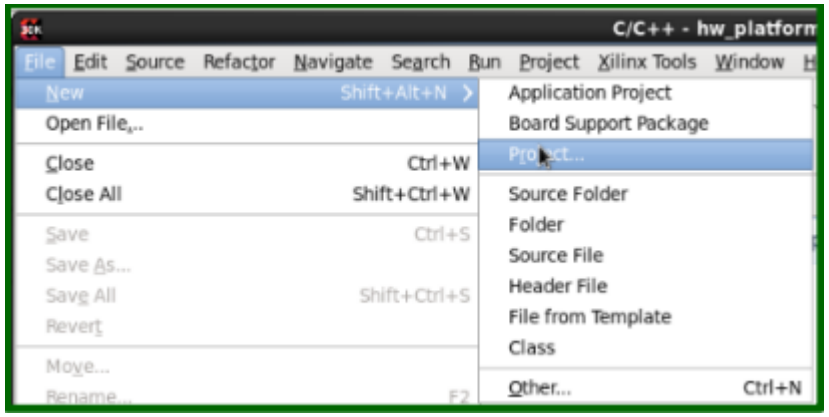
Tworzenie FSBL.elf

- Uruchamiamy Vivado dzięki komendzie w terminalu: vivado
- Otwieramy projekt dostępny z prezentacją.
- Eksportujemy zaprojektowany projekt sprzętu do aplikacji SDK.

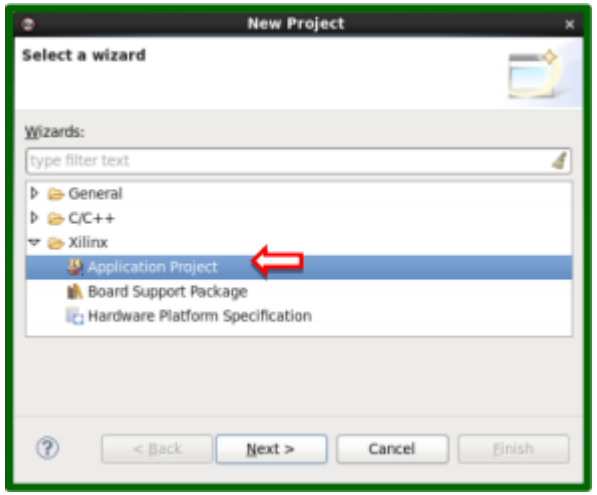


Tworzenie FSBL.elf

- Tworzymy nowy projekt:

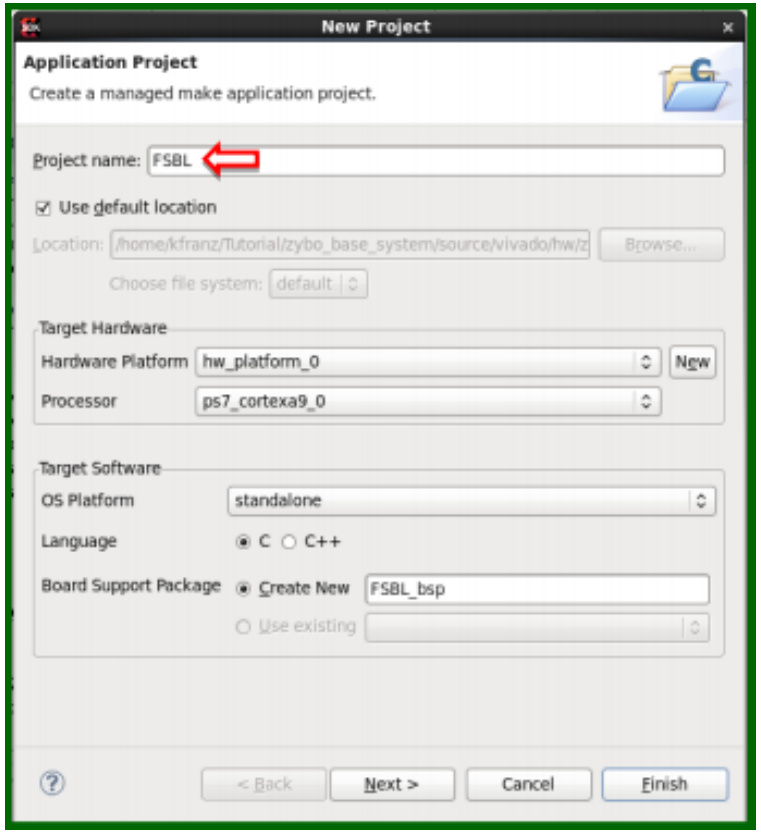


- Wybieramy opcję Application Project



Tworzenie FSBL.elf

- Wypełniamy okno jak w poniższym screenie:
- Klikamy *Next* > i przechodzimy do końcowego okna w którym wybieramy opcję *Zynq FSBL*.



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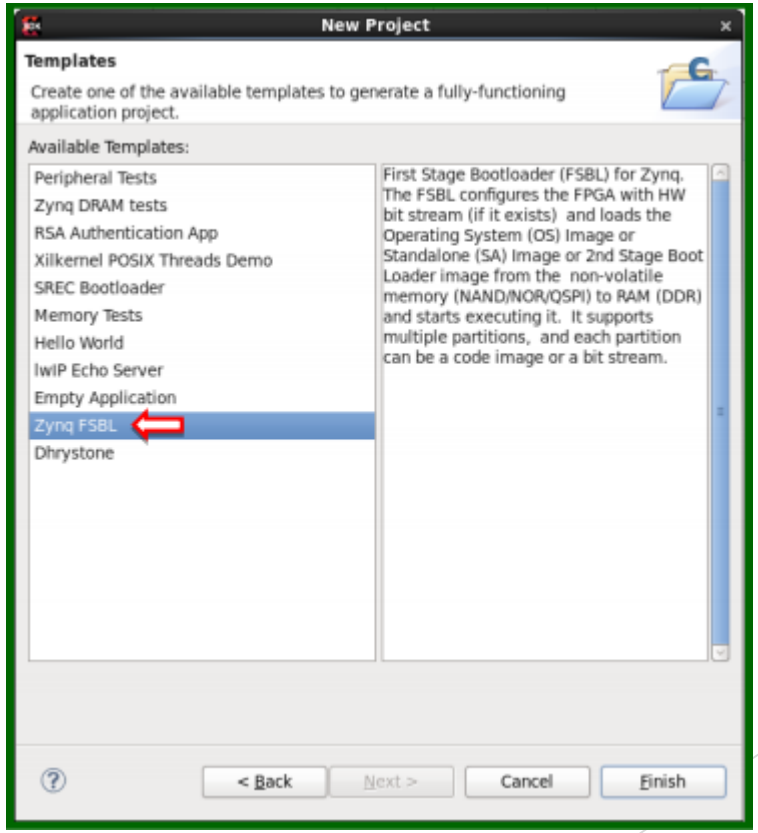
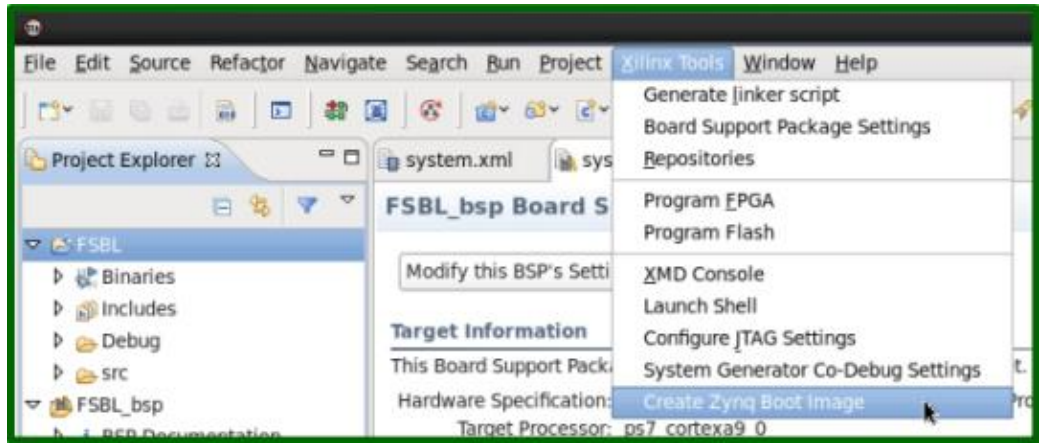
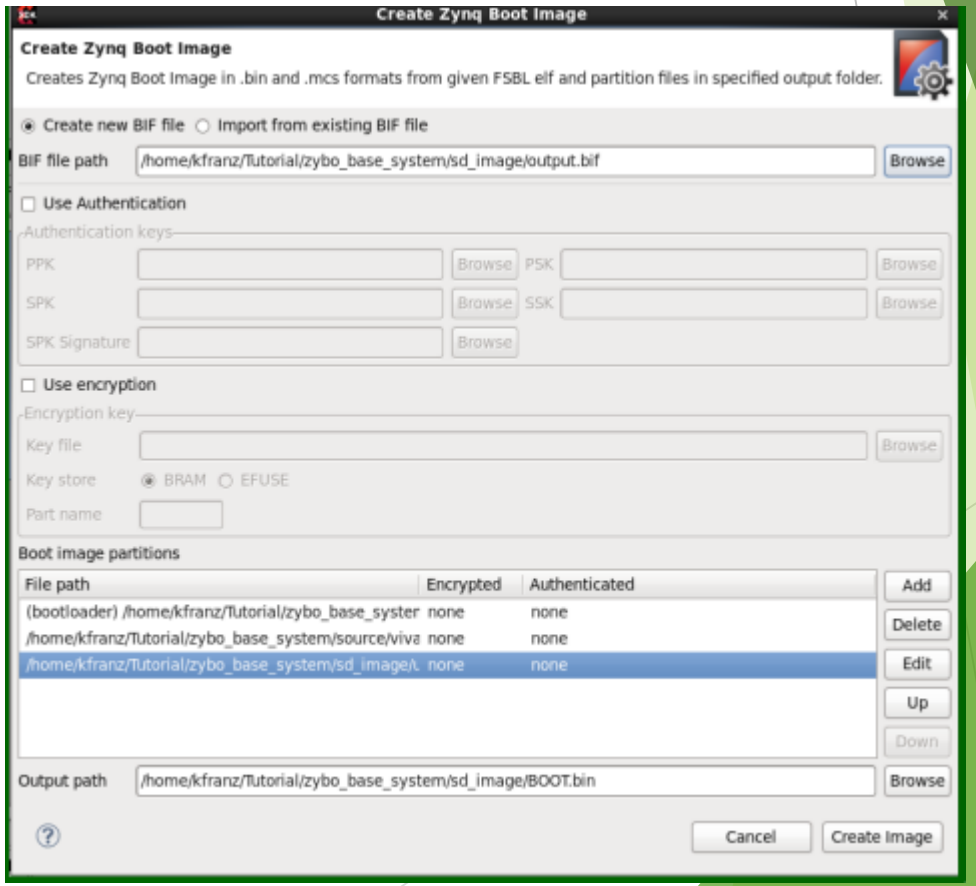


Tworzenie BOOT.bin

- W SDK uruchamiamy *Xilinx Tools ->Create Zynq Boot Image*
- *W otwartym oknie dodajemy pliki potrzebne do zbudowania pliku BOOT.bin*
  - *FSBL.elf - ustawiony jako bootloader*
  - *u-boot.elf*
  - *System.bit*





Tworzenie devicetree.dtb

- W plikach dostępnych z projektem znajduje się plik zynq-ZYBO.dts oraz folder *dtc*.
- Kompilacja pliku devicetree.dtb:

- mkdir devicetree
- cd decivetree
- mkdir dts
- cp –r ../dtc ../devicetree
- cp ../zynq-ZYBO.dts ..devicetree/dts
- dtc/dtc –I dts –0 dtb -o ./devicetree.dtb dts/zynq-ZYBO.dts